Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	14	"6711411".pn. "6134234".pn. "5398317".pn. "5907685".pn. "6748451".pn. "5875179".pn. "5892957".pn.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/13 15:21
L3	791	703/14.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/13 15:21
L4	188	703/16.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/13 15:21
L5	198	703/17.ccls.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/13 15:21
L6	153	(distributed same architecture same simulation)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2005/06/13 15:43
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1 Corolla partitioning for distributed logic simulation of VLSI-circuits

Christian Sporrer, Herbert Bauer

July 1993 **ACM SIGSIM Simulation Digest , Proceedings of the seventh workshop on Parallel and distributed simulation**, Volume 23 Issue 1

Full text available: pdf(730.67 KB) Additional Information: full citation, abstract, references, citings, index terms

Time Warp has evolved to a common technique for distributed simulation. Speedup in Time Warp simulation systems mainly depends on two overhead factors: first, the load on the simulators has to be well balanced and second, communication and rollbacks have to be kept to a minimum. Both of these factors are influenced by the partitioning of the simulated system. In this paper, we focus on various static partitioning schemes used to partition digital circuits for distributed simulation. < ...

2 Exploiting temporal independence in distributed preemptive circuit simulation

P. Walker, S. Ghosh

March 1997 **Proceedings of the 1997 European conference on Design and Test**

Full text available: pdf(596.77 KB) Additional Information: full citation, abstract

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In digital circuit simulation hidden opportunities for concurrent execution of models often exist, arising from the propagation delay associated with the generation of output events by the circuit models. An event prediction algorithm is developed to identify such parallelism, increasing the simulation execution rate. The algorithm uses an event prediction network and simulates circuits asynchronously and deadlock free, while honoring the preemptive semantics associated with digital circuit simu ...

Keywords: asynchronous simulation, circuit analysis computing, concurrent execution, digital circuit simulation, distributed preemptive circuit simulation, event prediction algorithm, output events, preemptive semantics, propagation delay, simulation execution rate, temporal independence

3 Session 10A: power analysis and optimization: Simulation and optimization of the power distribution network in VLSI circuits

G. Bai, S. Bobba, I. N. Hajj

November 2000 **Proceedings of the 2000 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(1.38 MB) Additional Information: full citation, abstract, references, citings

In this paper, we present simulation techniques to estimate the worst-case voltage variation using a RC model for the power distribution network. Pattern independent maximum envelope currents are used as a periodic input for performing the frequency-domain steady-state simulation of the linear RC circuit to evaluate the worst-case instantaneous voltage drop for the RC power distribution networks. The proposed technique unlike existing techniques, is guaranteed to give the maximum voltage drop at ...

4 Parallel logic level simulation of VLSI circuits

Rajive Bagrodia, Zheng Li, Vikas Jha, Yuan Chen, Jason Cong

December 1994 **Proceedings of the 26th conference on Winter simulation**

Full text available: pdf(755.69 KB) Additional Information: full citation, references, citings, index terms

5 Parallel gate-level circuit simulation on shared memory architectures

Rajive Bagrodia, Yu-an Chen, Vikas Jha, Nicki Sonpar

July 1995 **ACM SIGSIM Simulation Digest , Proceedings of the ninth workshop on Parallel and distributed simulation**, Volume 25 Issue 1

Full text available: pdf(874.12 KB) Additional Information: full citation, abstract, references, index terms

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This paper presents the results of an experimental study to evaluate the effectiveness of parallel simulation in reducing the execution time of gate-level models of VLSI circuits. Specific contributions of this paper include (i) the design of a gate-level parallel simulator that can be executed, without any changes on both distributed memory and shared memory parallel architectures, (ii) demonstrated speedups with both conservative and optimistic simulation protocols (almost all previous st ...

Keywords: ISCAS85 benchmark suite, Sparc1000, VLSI, VLSI circuits, circuit analysis computing, digital simulation, execution time, gate-level parallel simulator, logic CAD, logic design, optimistic simulation protocols, parallel gate-level circuit simulation, parallel programming, parallel simulation, shared memory architectures, shared memory systems

6 Conservative circuit simulation on shared-memory multiprocessors

Jörg Keller, Thomas Rauber, Bernd Rederlechner

July 1996 **ACM SIGSIM Simulation Digest , Proceedings of the tenth workshop on Parallel and distributed simulation**, Volume 26 Issue 1

Full text available: pdf(890.97 KB) Additional Information: full citation, abstract, references, citings, index terms

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We investigate conservative parallel discrete event simulations for logical circuits on shared-memory multiprocessors. For a first estimation of the possible speedup, we extend the critical path analysis technique by partitioning strategies. To incorporate overhead due to the management of data structures, we use a simulation on an ideal parallel machine (PRAM). This simulation can be directly executed on the SB-PRAM prototype, yielding both an implementation and a basis for data structure optim ...

Keywords: circuit simulation, conservative simulation, multiprefix operation, parallel random access machine (PRAM), shared memory multiprocessor, speedup

estimation

7 Evaluating the use of pre-simulation in VLSI circuit partitioning

Roger D. Chamberlain, Cheryl D. Henderson

July 1994 **ACM SIGSIM Simulation Digest , Proceedings of the eighth workshop on Parallel and distributed simulation**, Volume 24 Issue 1

Full text available: pdf(562.59 KB) Additional Information: full citation, abstract, references, citings, index terms

One of the significant difficulties in partitioning logic circuits for distributed simulation is the lack of a priori knowledge concerning the evaluation frequency of individual circuit elements. A number of researchers have resorted to pre-simulation to estimate these evaluation frequencies. In this paper we empirically investigate the wisdom of relying on pre-simulation results, and evaluate the degree to which early evaluation frequencies predict later evaluation frequencies. The results ...

8 An improved cost function for static partitioning of parallel circuit simulations using a conservative synchronization protocol

Kevin L. Kapp, Thomas C. Hartrum, Tom S. Wailes

July 1995 **ACM SIGSIM Simulation Digest , Proceedings of the ninth workshop on Parallel and distributed simulation**, Volume 25 Issue 1

Full text available: pdf(1.24 MB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Distributing computation among multiple processors is one approach to reducing simulation time for large VLSI circuit designs. However, parallel simulation introduces the problem of how to partition the logic gates and system behaviors of the circuit among the available processors in order to obtain maximum speedup. A complicating factor that is often ignored is the effect of the time-synchronization protocol (conservative [1] or optimistic [2]). Inherent in the partitioning problem is the ...

Keywords: VLSI circuit design, circuit analysis computing, conservative synchronization protocol, discrete event simulation, graph-based partitioning tool, logic CAD, logic partitioning, objective cost function, parallel circuit simulations, parallel programming, parallel simulation, static partitioning, synchronization protocol, time-synchronization protocol

9 A multidimensional study on the feasibility of parallel switch-level circuit simulation

Yu-an Chen, Vikas Jha, Rajive Bagrodia

June 1997 **ACM SIGSIM Simulation Digest , Proceedings of the eleventh workshop on Parallel and distributed simulation**, Volume 27 Issue 1

Full text available: pdf(1.19 MB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

This paper presents the results of an experimental study to evaluate the effectiveness of multiple synchronization protocols and partitioning algorithms in reducing the execution time of switch-level models of VLSI circuits. Specific contributions of this paper include: (i) parallelizing an existing switch-level simulator such that the model can be executed using conservative and optimistic simulation protocols with minor changes, (ii) evaluating effectiveness of several partitioning algorithms ...

10 A statistical performance simulation methodology for VLSI circuits

Michael Orshansky, James C. Chen, Chenming Hu

May 1998 **Proceedings of the 35th annual conference on Design automation - Volume 00**

Full text available: pdf(243.16 KB) Additional Information: full citation, abstract, references, citings, index terms

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A statistical performance simulation (SPS) methodology for VLSI circuits is presented. Traditional methods of worst-case corner analysis lack accuracy and Monte-Carlo simulations cannot be applied to VLSI circuits because of their complexity. SPS methodology is accurate because no statistical information about the device parameter variation is lost. It achieves efficiency by analyzing the smaller circuit blocks and generating the performance distribution for the entire circuit. Circuit eval ...

Keywords: custom sizing, migration, timing optimazation

11 Parallel and distributed discrete event simulation: algorithms and applications

Richard M. Fujimoto

December 1993 **Proceedings of the 25th conference on Winter simulation**

Full text available: pdf(1.02 MB) Additional Information: full citation, references, citings

12 Electromagnetic modeling and signal integrity simulation of power/ground networks in high speed digital packages and printed circuit boards

Frank Y. Yuan

May 1998 **Proceedings of the 35th annual conference on Design automation - Volume 00**

Full text available: pdf(275.46 KB) Additional Information: full citation, abstract, references, index terms

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The electromagnetic modeling and parameter extraction of digital packages and PCB boards for system signal integrity applications are presented. A systematic approach to analyze complex power/ground structures and simulate their effects on digital systems is developed. First, an integral equation boundary element algorithm is applied to the electromagnetic modeling of the PCB structures. Then, equivalent circuits of the power/ground networks are extracted from the EM solution. In an integra ...

Keywords: custom sizing, migration, timing optimazation

13 Fault simulation in a distributed environment

Patrick A. Duba, Rabindra K. Roy, Jacob A. Abraham, William A. Rogers

June 1988 **Proceedings of the 25th ACM/IEEE conference on Design automation**

Full text available: pdf(776.82 KB) Additional Information: full citation, abstract, references, citings, index terms

Fault simulation of VLSI circuits takes considerable computing resources and there have been significant efforts to speed up the fault simulation process. This paper describes a distributed fault simulator implemented on a loosely-coupled network of general purpose computers. The techniques used result in a close to linear speedup and can be used effectively in most industrial VLSI CAD environments.

14 Simulation methods for RF integrated circuits

Ken Kundert

November 1997 **Proceedings of the 1997 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(97.56 KB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

The principles employed in the development of modern RF simulators are introduced and the various techniques currently in use, or expected to be in use in the next few years, are surveyed. Frequency and time domain techniques are presented and contrasted, as are steady state and envelope techniques and large and small signal techniques.

Keywords: RF integrated circuits, envelope techniques, integrated circuit modelling, modern RF simulators, simulation methods, small signal techniques, state techniques, time domain techniques

15 Parallel timing simulation on a distributed memory multiprocessor

Chih-Po Wen, Katherine A. Yelick

November 1993 **Proceedings of the 1993 IEEE/ACM international conference on Computer-aided design**

Full text available: pdf(652.49 KB) Additional Information: full citation, references, citings

16 Characterization of parallelism and deadlocks in distributed digital logic simulation

L. Soule, A. Gupta

June 1989 **Proceedings of the 26th ACM/IEEE conference on Design automation**

Full text available: pdf(835.68 KB) Additional Information: full citation, abstract, references, citings, index terms

This paper explores the suitability of the Chandy-Misra algorithm for digital logic simulation. We use four realistic circuits as benchmarks for our analysis, with one of them being the vector-unit controller for the Titan supercomputer from Ardent. Our results show that the average number of logic elements available for concurrent execution ranges from 10 to 111 for the four circuits, with an overall average of 68. Although this is twice as much parallelism as that obtained by traditional ...

17 DVS: An Object-Oriented Framework for Distributed Verilog Simulation

Lijun Li, Hai Huang, Carl Tropper

June 2003 **Proceedings of the seventeenth workshop on Parallel and distributed simulation**

Full text available: pdf(161.05 KB) Publisher Site Additional Information: full citation, abstract, citings, index terms

There is a wide-spread usage of hardware design languages(HDL) to speed up the time-to-market for the designof modern digital systems. Verification engineers can simulatehardware in order to verify its performance and correctnesswith help of an HDL. However, simulation can'tkeep pace with the growth in size and complexity of circuitsand has become a bottleneck of the design process. DistributedHDL simulation on a cluster of workstations hasthe potential to provide a cost-effective solution to th ...

18 A unified modeling methodology for performance evaluation of distributed discrete event simulation mechanisms

Bruno R. Preiss, Wayne M. Loucks, V. Carl Hamacher

December 1988 **Proceedings of the 20th conference on Winter simulation**

Full text available: pdf(1.05 MB) Additional Information: full citation, abstract, references, index terms

The main problem associated with comparing distributed discrete event simulation mechanisms is the need to base the comparisons on some common problem specification. This paper presents a specification strategy and language which allows the same simulation problem specification to be used for both distributed discrete event simulation mechanisms as well as the traditional single event list mechanism. This paper includes: a description of the Yaddes specification language; a description of t ...

19 Distributed and parallel demand driven logic simulation

K. Subramanian, M. R. Zargham

January 1991 **Proceedings of the 27th ACM/IEEE conference on Design automation**

Full text available: pdf(583.13 KB) Additional Information: full citation, abstract, references, citings, index terms

Based on the demand-driven approach, distributed and parallel simulation algorithms are proposed. Demand-driven simulation tries to minimize the number of component computations by performing only those required for the watched output requests. For a specific output value request, the input line values that are required are requested from the related component. The process continues until known system input signal values are requested. We present a distributed demand-driven algorithm with a ...

20 Maximum voltage variation in the power distribution network of VLSI circuits with RLC models

Sudhakar Bobba, Ibrahim Hajj

August 2001 **Proceedings of the 2001 international symposium on Low power electronics and design**

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